

# AI in Critical Avionics Certification and Embedded Challenges

**Adrien Gauffriau**  
*Embedded AI Expert - Airbus*

***ECRTS 2024 - Lille - Industrial Keynote***



# AGENDA

Airbus challenges

Certification of Artificial Intelligence

Convolutional Neural Networks computing





# AGENDA

## Airbus challenges

Certification of Artificial Intelligence

Convolutional Neural Networks computing

# We pioneer sustainable aerospace for a safe and united world

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Leading the journey  
towards clean  
aerospace

Helping  
customers defend  
their values

Connecting and uniting  
people across the  
globe



# Safety first, in everything we do

**Safe**

Aircraft

**Safety**

Operated

**Safe**

Air Transport  
System

Safety is the foundation of our business at Airbus, and encompasses all activities to prevent incidents and accidents involving Airbus products and services, to manage such events when they occur, to draw lessons learned and implement change as appropriate.

# Leading sustainable aviation

2030

- Offer up to **100% SAF capability** on our commercial aircraft

2035

- Be the **1<sup>st</sup> major manufacturer** to offer a hydrogen-powered aircraft

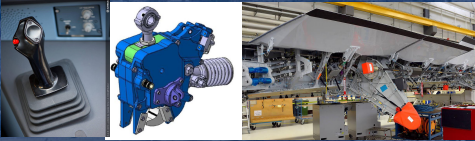
2050

Reach '**net-zero carbon emissions**' by 2050



# Embedded Systems are bringing Aircraft Differentiation

Flight controls



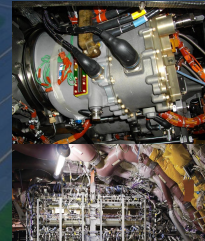
Environmental control



Cockpit operations & Systems



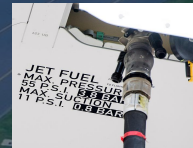
Electrical system



Landing gears



Fuel management





# Avionics Example : 4 Generations have converged on A350 standard

## 1 Early Commercial Jets



## 2 More auto-flight systems



## 3 Glass Cockpit



## 4 Fly-by-Wire





## Software brings product DIFFERENTIATION !



# And Tomorrow... : Certifiable & Embedded AI



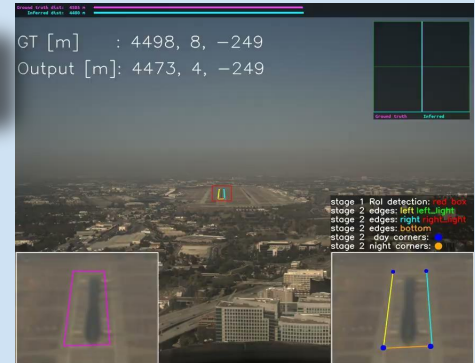
- AI used as a safety net

Improve  
Safety

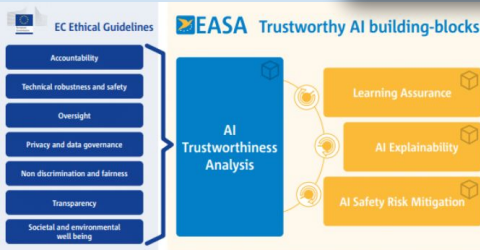
Extend  
Operational domain

Embedded AI

Ensure  
Certification



- AI improves sensors technol



- Demonstrate the intended behavior
- Keep the semantics of the trained model



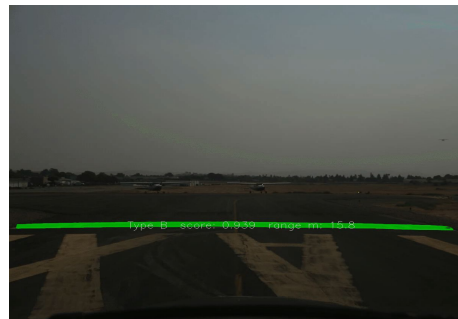
## Many vision applications ...



Assisted taxi



Obstacle detection



Runway incursion detection



Auto-take-off

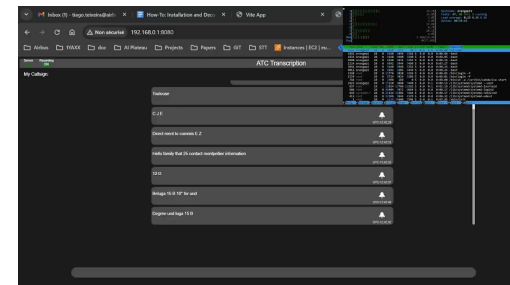


Autoland



Pilot monitoring

... but also natural language processing



ATC speech-to-text

... and more to come !

## ATC Transcription

**My Callsign:**

Toulouse

CJE

UTC-12:42:29

Direct ment to commis EZ

UTC-12:42:31

Hello family that 25 contact montpellier information

UTC-12:42:35

12 D

UTC-12:42:37

Beluga 15 B 10° for und

UTC-12:42:40

Degree und Jahr 15 B

100-124242



# What are at stakes ?

Airbus Amber





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# IMPACT ON CURRENT SYSTEM DEVELOPMENT

```
Dim x As Integer
Dim TempResult As String
Dim ActualIterations As Integer

*Loop As needed
For x = 1 To Iterations
  ActualIterations += 1
  If Deep Then
    While Not Finished
      DeepCopy(x)
    End While
  Else
    If Finished Then
      ShallowCopy
    End If
  Next x
End Function

ByVal x As Integer
x = 48
x = 57

Dim x As Integer
Dim y As Integer
Dim z As Integer
Dim w As Integer
Dim v As Integer
Dim u As Integer
Dim t As Integer
Dim s As Integer
Dim r As Integer
Dim q As Integer
Dim p As Integer
Dim o As Integer
Dim n As Integer
Dim m As Integer
Dim l As Integer
Dim k As Integer
Dim j As Integer
Dim i As Integer
Dim h As Integer
Dim g As Integer
Dim f As Integer
Dim e As Integer
Dim d As Integer
Dim c As Integer
Dim b As Integer
Dim a As Integer
```

For decades!

Systems based on  
imperative software

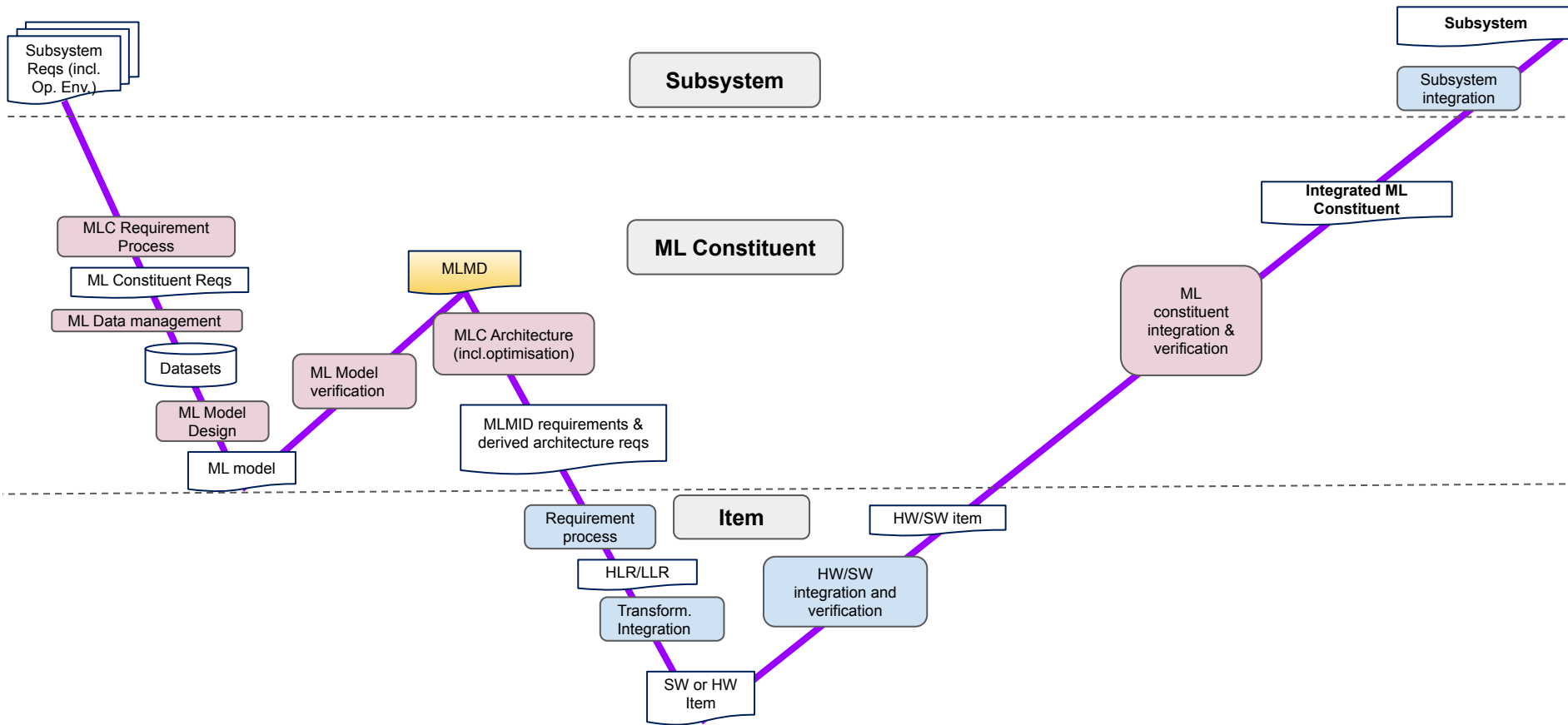


Design  
from  
SS

# ARP6983/ED-324 : W development cycle

MLMD: ML Model Description  
MLMID: ML Model Item Description  
MLC: ML Constituent

ARP6983/ED-324  
Existing standard





# ARP6983/ED-324 : W development cycle

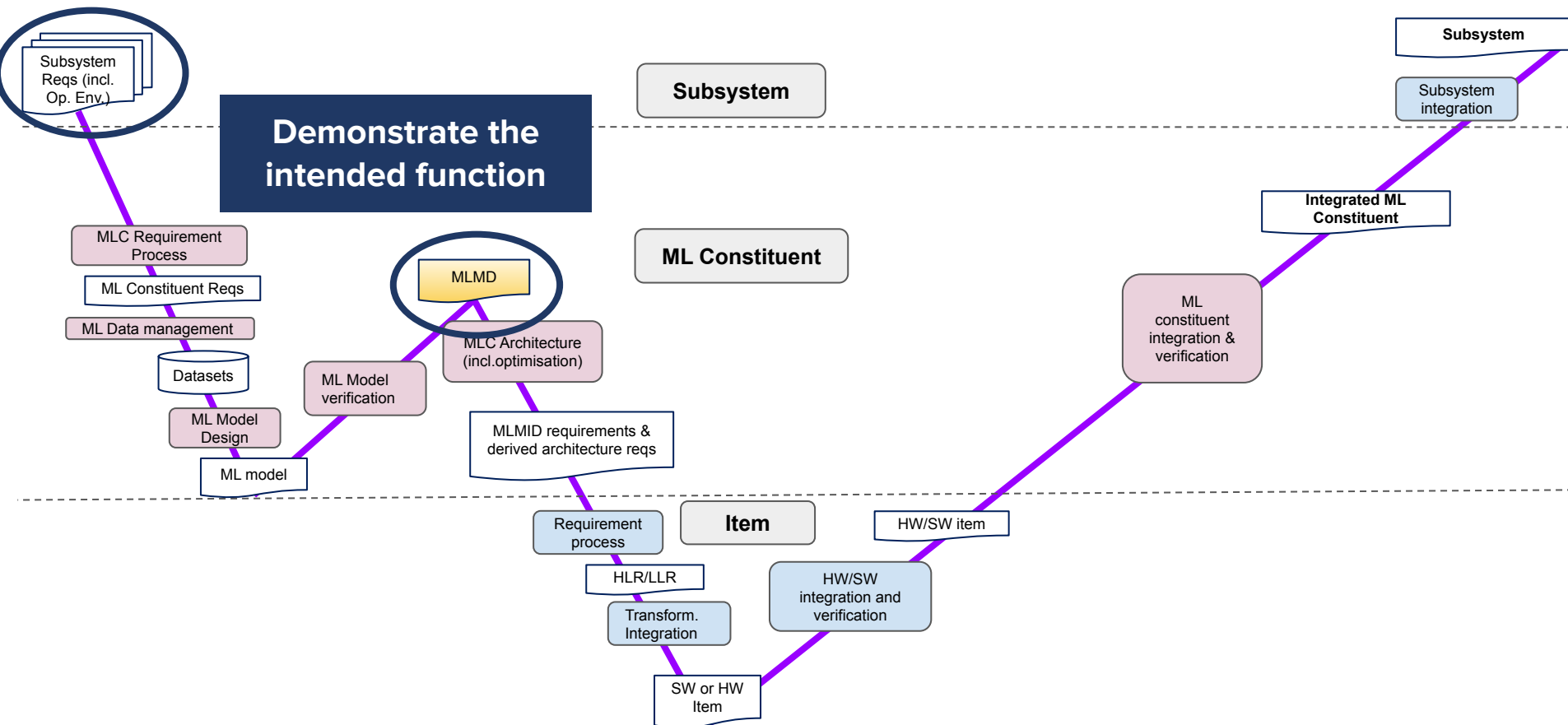
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# ARP6983/ED-324 : W development cycle

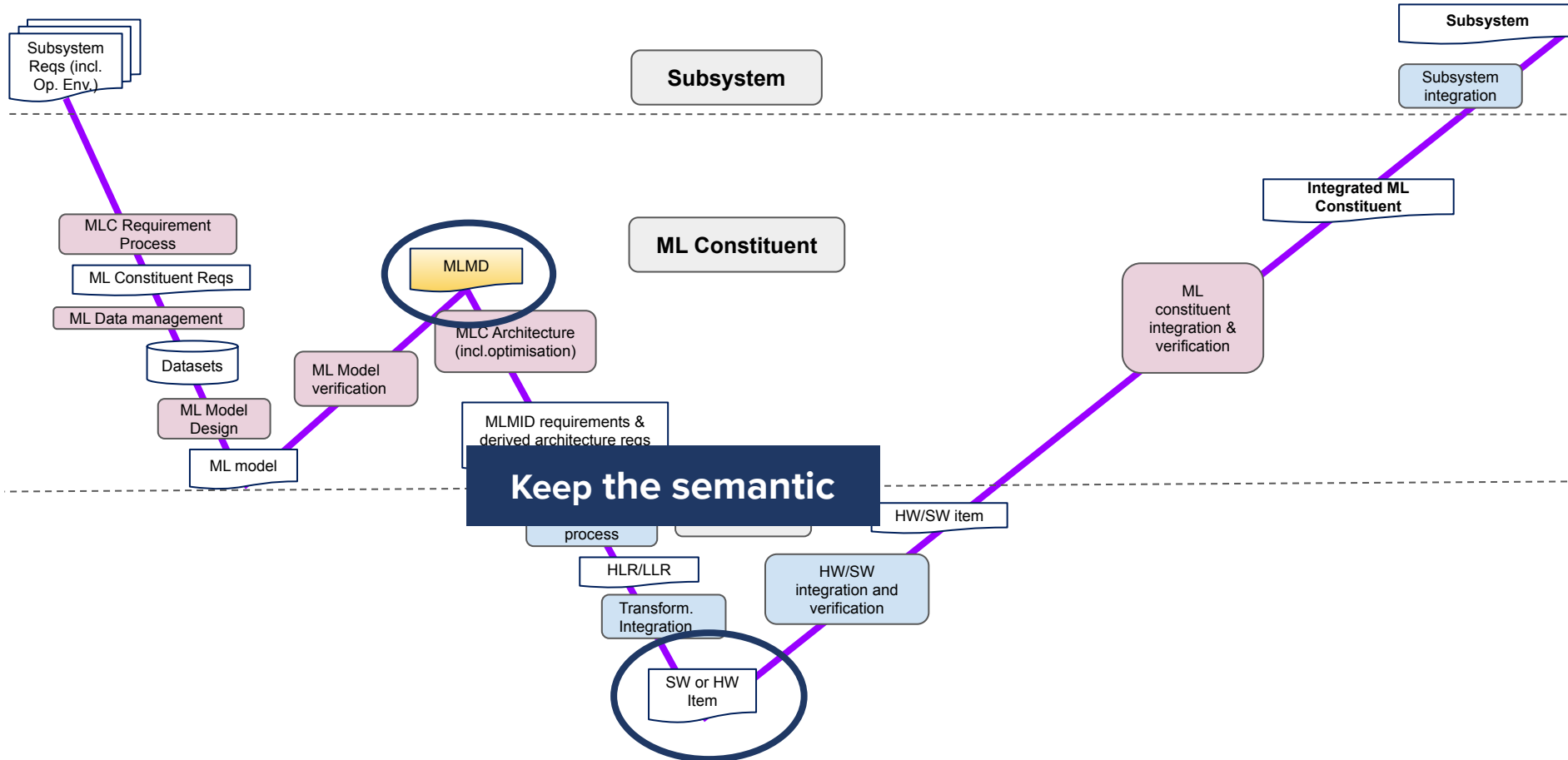
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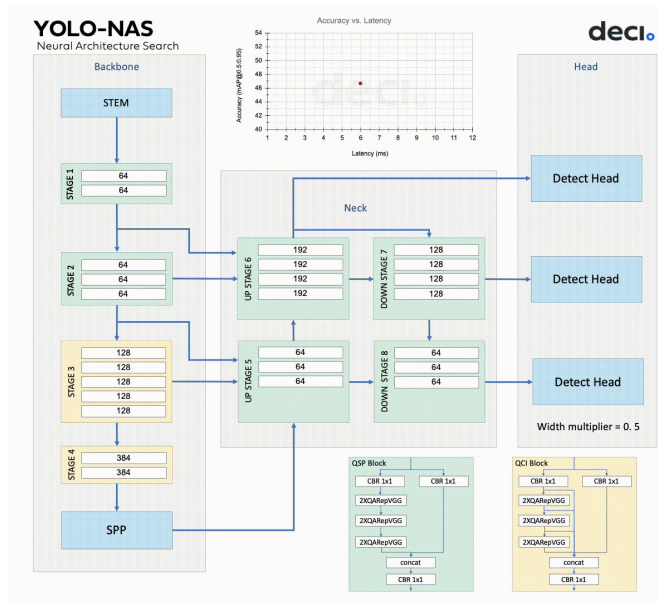
ARP6983/ED-324

Existing standard



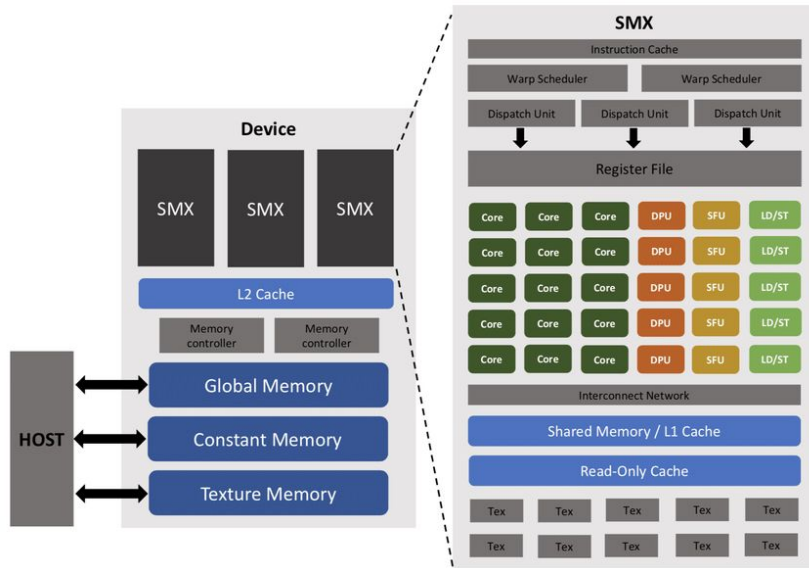


# ARP6983/ED-324 : W development cycle



YoloNAS Neural Network  
Architecture

+



Typical GPU architecture

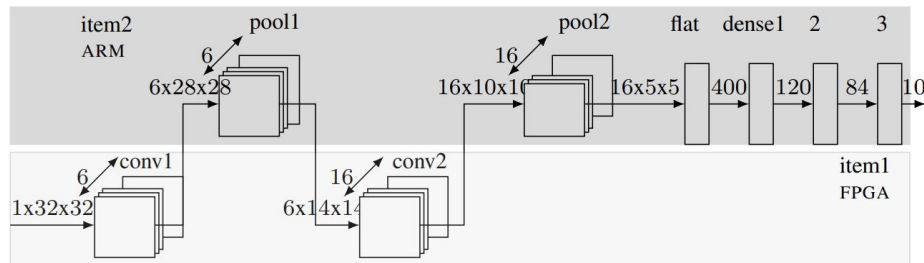
=

Inference Model on target

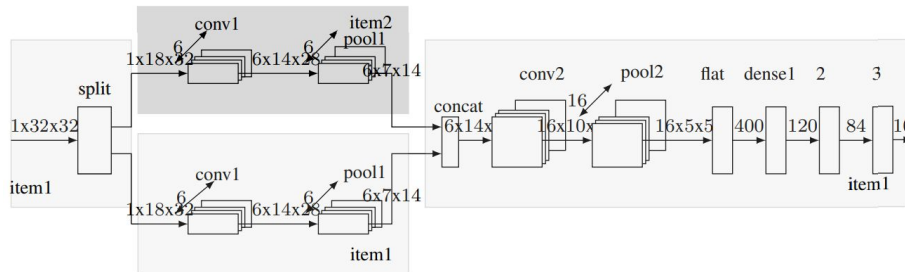
We need to express mapping between  
Neural Networks logics and HW resources

# What we would like to express

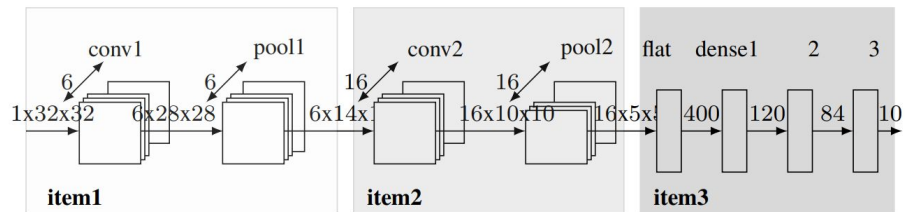
## Offloading of layers



## Parallelization inside layers



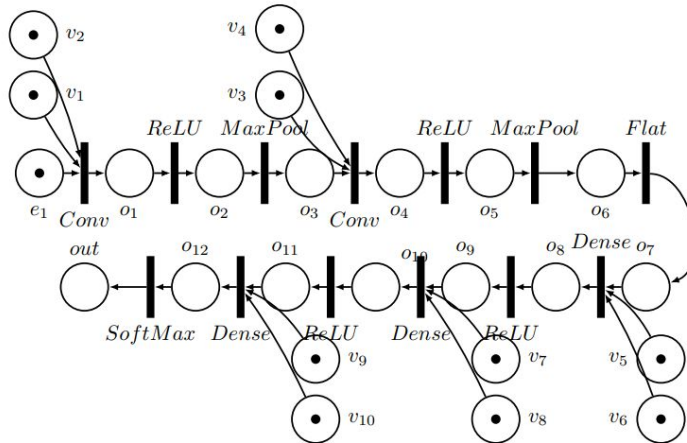
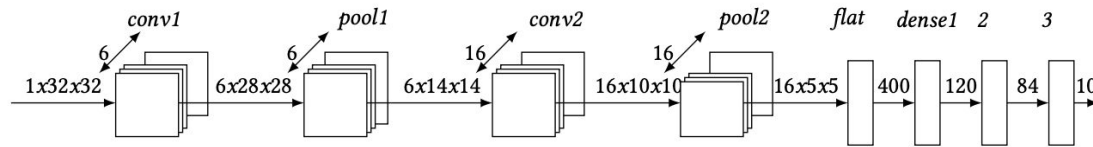
## Pipelining





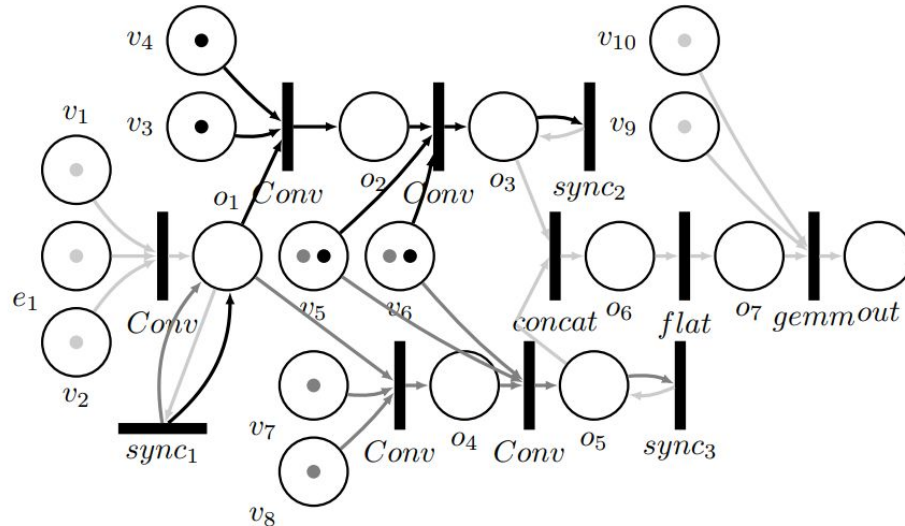
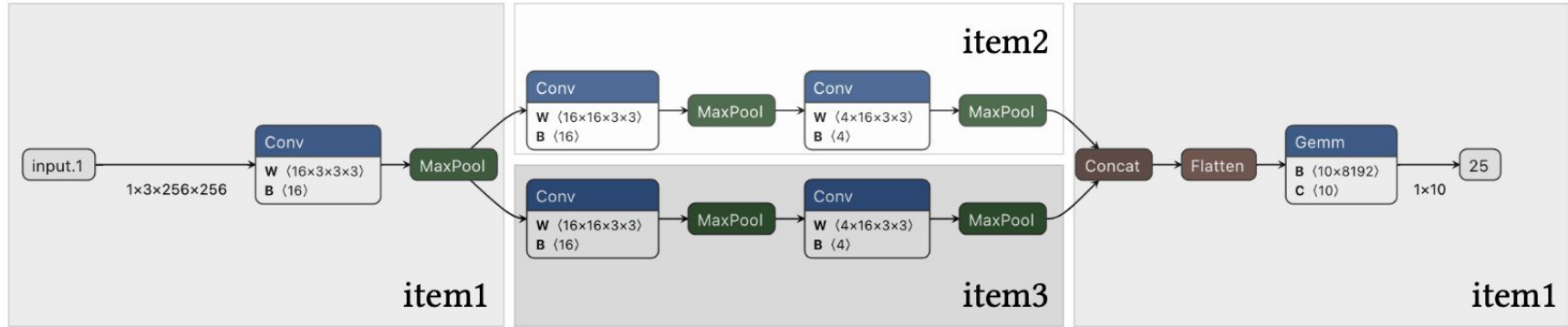
# Neural Networks semantics with PetriNet

- Split the initial neural network
- Demonstrate that the union of splits is equal to the initial function



Expression of **all possible** execution orders

# Multi-Items with colored Petri-Nets



- ERTS 2024 publication
- ONNX working group - Safety Critical profile

## Paper

Formal description of ML models for unambiguous implementation

Adrien Gauffriaux, Iryna De Albuquerque Silva, Claire Pagetti





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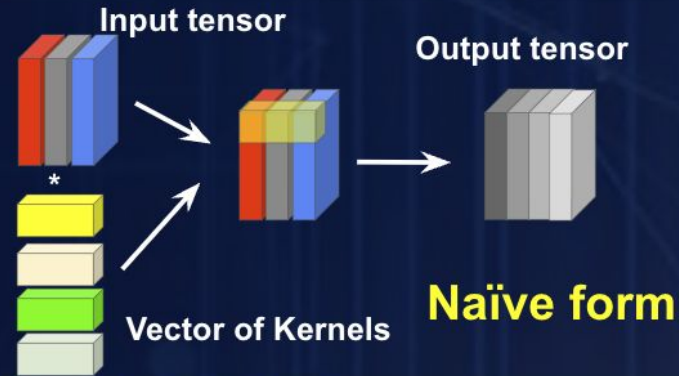
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Convolutional Neural Networks computing

# Convolution is “just” a matrix multiplication

## Computing a convolution layer



```
int inference(double prediction[1], double nn_input[27]){
    ...
    // Conv2D_1
    for (int f = 0; f < 5; ++f){
        for (int i = 0; i < 2; ++i){
            for (int j = 0; j < 2; ++j){
                sum = 0;
                for (int c = 0; c < 3; ++c){
                    for (int m = 0; m < 2; ++m){
                        for (int n = 0; n < 2; ++n){
                            int ii = i*1 + m*1 - 0;
                            int jj = j*1 + n*1 - 0;
                            if (ii >= 0 && ii < 3 && jj >= 0 && jj < 3){
                                sum += output_pre[(ii*3 + jj)*3 + c] * weights_Conv2D_01[(m*2 + n)*3 + c]*5 + f];
                            }
                        }
                    }
                }
                sum += biases_Conv2D_01[f];
                output_cur[(i*2 + j)*5 + f] = sum > 0 ? sum : 0;
            }
        }
    }
}
```

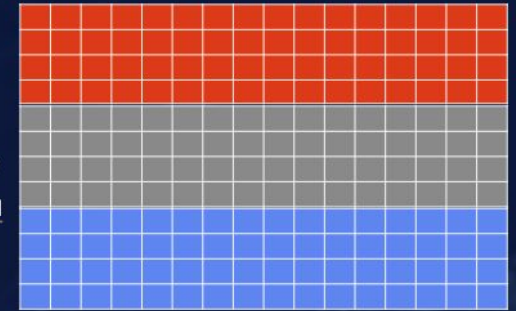
$$\sum_{m=1}^{f_h} \sum_{n=1}^{f_w} \sum_{c=1}^{f_c} K_{m,n,c}^z \times I_{(i-1) \times s_h + m, (j-1) \times s_w + n, c}$$

## Matrix form

Input tensor



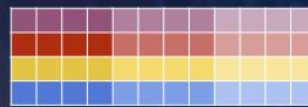
image2col



Kernels

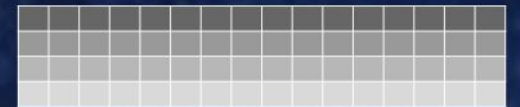


Kernel2row



Matrix A : Kernels

Matrix C : Convolution outputs

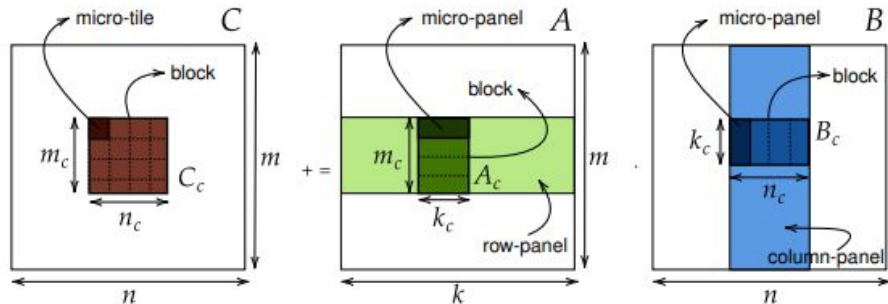


$$C = A.B$$



# Develop a certifiable code intensive and efficient computation

- Plenty of BLAS library
- BUT**
- Worst case execution time is mandatory
- Efficient utilization of resources



Rationale for the PhD of Iryna De albuquerque

ACETONE is a solution for CPU implementation based on blocked matrix multiplication

Extension to more complex hardware in progress

## Papers

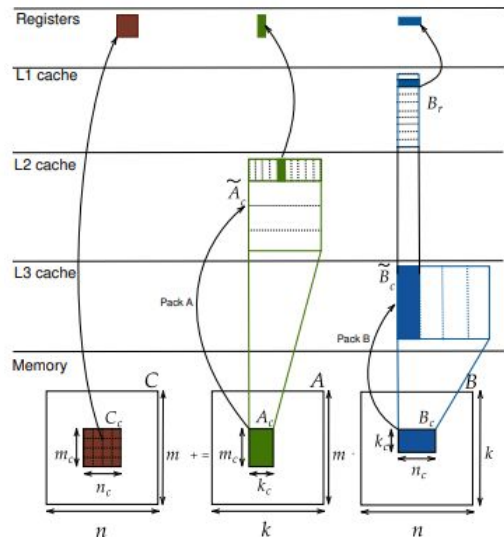
A Predictable SIMD Library for GEMM Routines. RTAS 2024: 55-67

Iryna De Albuquerque Silva, Thomas Carle, Adrien Gauffriau, Victor Jégu, Claire Pagetti

ACETONE: Predictable Programming Framework for ML Applications in Safety-Critical Systems.

ECRTS 2022: 3:1-3:19

Iryna De Albuquerque Silva, Thomas Carle, Adrien Gauffriau, Claire Pagetti::



# Computation needed

Typical Use case for aeronautics requires 1 Tera Floating Point Operation per second (1 TFLOPS)

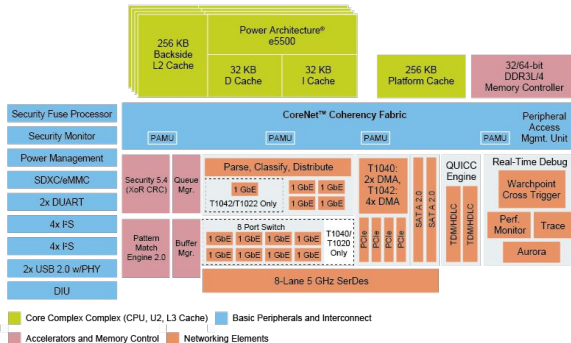


**1,0 GHz**

**4 FPU's => 4 GFLOPS**

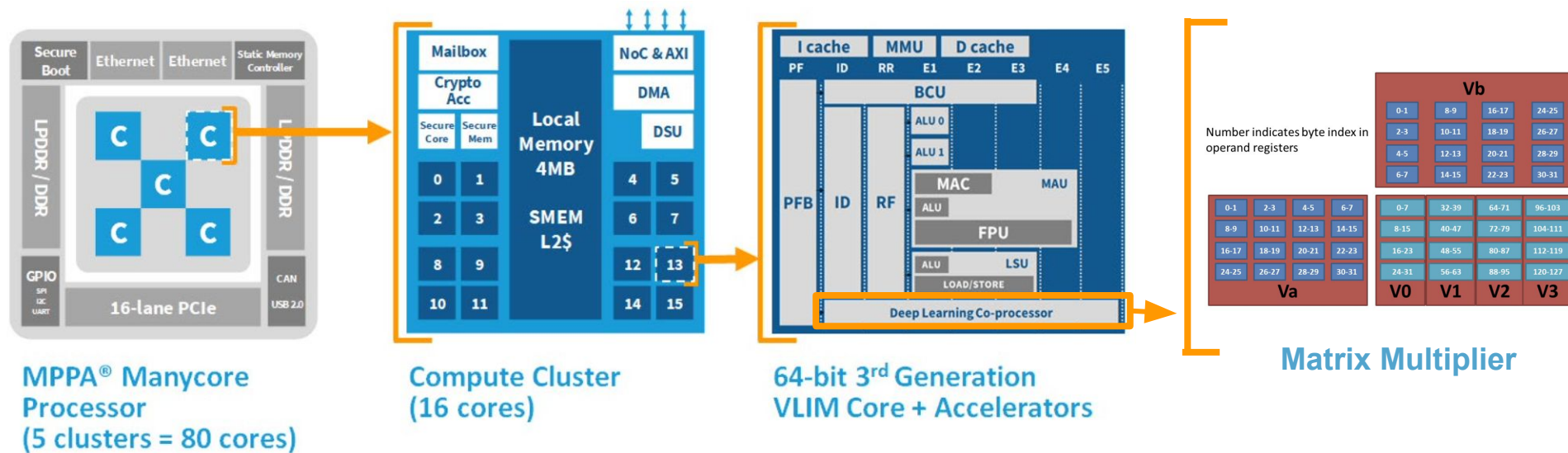
Increase of the frequency is not possible

**Chip Makers increase number of ALUs/FPUs**



Integration/Aggregation of the ALUs/FPUs is the crux

# Example of the Kalray MPPA

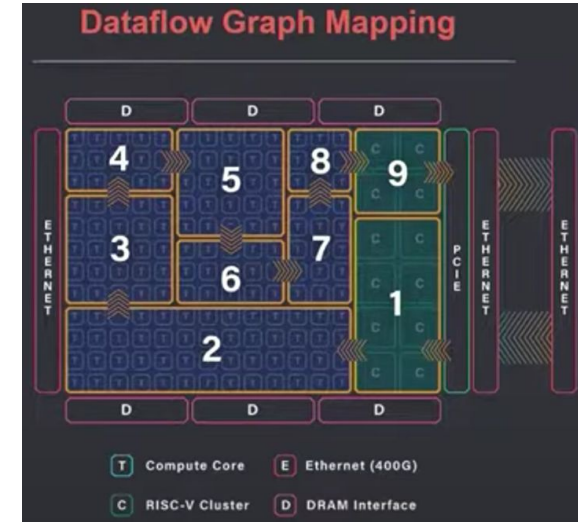
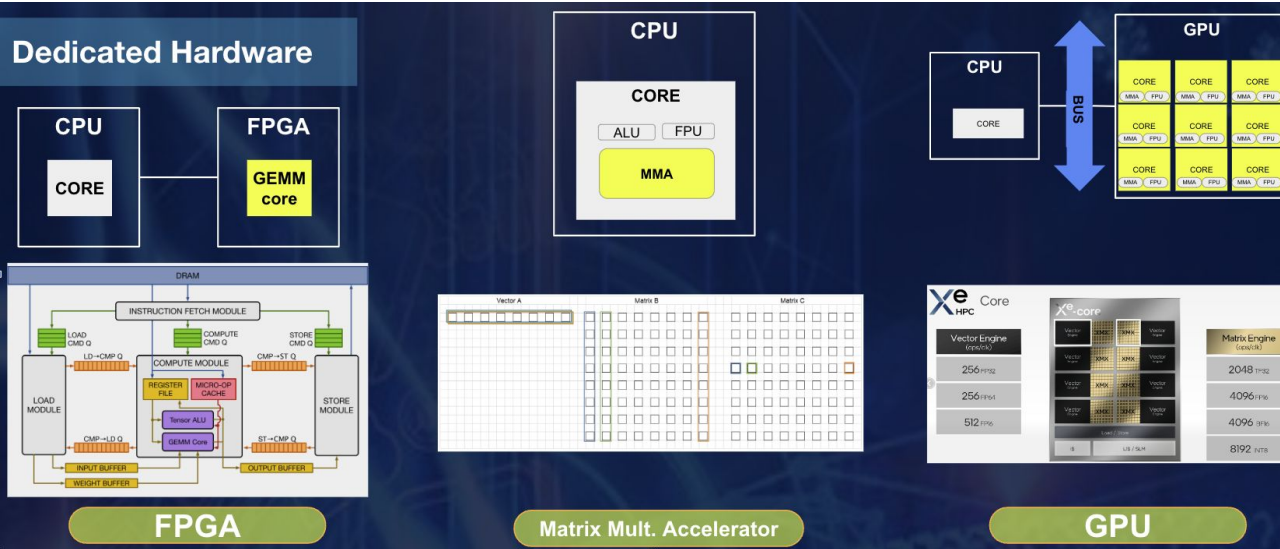


**80** Deep Learning Unit (DPU) - Each DPU has 16 FPU => 1280 FPUs

**1,280 TFLOPs @1GHz**



# Design space exploration



Allocation of compute units  
to part of the CNN  
*Tenstorrent company*

## BUT critical avionics consideration remains

- HW failure and impact on Neural Networks
- Sensitivity to SEU / MBU
- WhiteBox with capabilities to handle software Low Layer

### Paper on HW failures

Methodology for formal verification of hardware safety strategies using SMT.

To appear LB EMSOFT IEEE Embedded Systems Letters (ESL) 2024  
Anthony Faure-Gignoux, Kevin Delmas, Adrien Gauffriau, Claire Pagetti.



# CONCLUSION

- Artificial Intelligence is mandatory to support Airbus ambitions
- Certification will be in place **BEFORE** first application
- Maturity of hardware and associated toolchain remains low





Thanks for your attention

Q&A