

# Replacement Policies for a Function-based Instruction Memory: A Quantification of the Impact on Hardware Complexity and WCET Estimates

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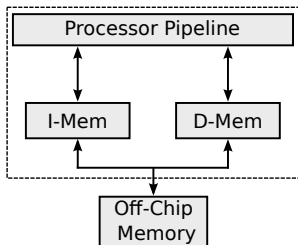
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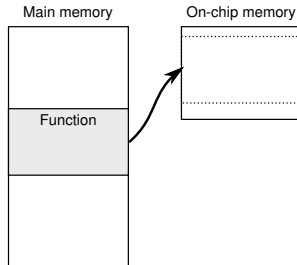
- ▶ Safety-critical hard real-time systems
  - ▶ No deadline miss tolerable
  - ▶ System schedule requires safe and tight WCET bound per task
- ▶ Determination of the timing of the whole system, including
  - ▶ the executed software (task with all input data sets, OS)
  - ▶ the underlying hardware (CPU, **memory hierarchy**, bus, etc.)
- ▶ Speed gap between processor and main memory
  - ▶ Usage of fast, but small on-chip memories

Memory hierarchy has a major contribution to the system's predictability and worst case performance



- ▶ Approaches for on-chip memories in hard real-time systems
  - ▶ Scratchpads with fixed content
  - ▶ SW-managed scratchpads
  - ▶ Cache locking
  - ▶ Cache analysis
  - ▶ **Function-based instruction memories**

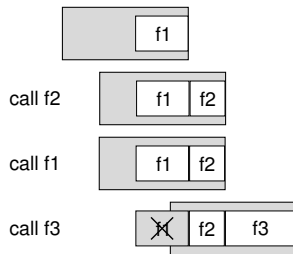
- ▶ Load a function completely into on-chip memory before executing
- ▶ Predictable and instantaneous execution of functions
- ▶ Examples:  
Method-Cache [Schoeberl 04]  
and D-ISP



Examination of the impact of different replacement policies on WCET estimate and hardware complexity

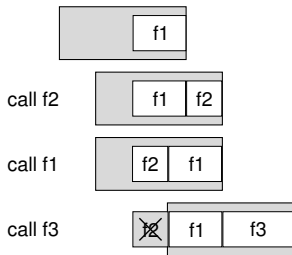
## FIFO replacement policy

- ▶ Keeping recently loaded functions
  - ▶ Eviction of the oldest function
- ▶ Implementable in hardware with low complexity
  - ▶ Queue with write and eviction pointer



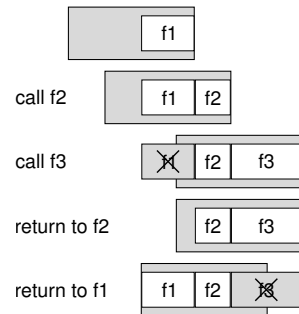
## LRU replacement policy

- ▶ Keeping frequently accessed functions
  - ▶ Eviction of the least recently used function
  - ▶ Order depends on access history
- ▶ Too complex to implement in hardware, because
  1. functions of different size
  2. reordering of memory content
  3. memory fragmentation

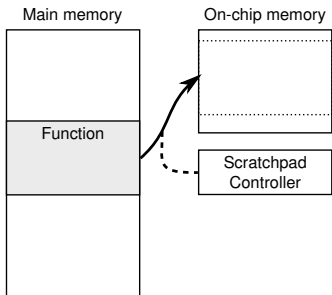


## Stack-based replacement policy

- ▶ Keep active branch of call tree
  - ▶ Definitely accessed again
  - ▶ At the expense of sibling function
  - ▶ Eviction of the function with largest stack distance
- ▶ Possible hardware implementation
  - ▶ Double ended queue with different write and eviction pointers for call and return



- ▶ Using function-based instruction memory D-ISP for comparison of the replacement policies

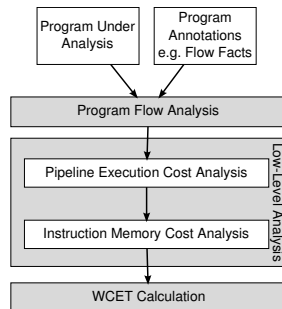


- ▶ Two operation phases:
  - load function & execute function
- ▶ Dynamic content management
  - ▶ Is aware of D-ISP content
  - ▶ Load of **complete function** from off-chip memory
  - ▶ A function is always in in memory before its execution
- ▶ Instruction memory access
  - ▶ **All fetches** directed to D-ISP
  - ▶ Always hit for any fetch

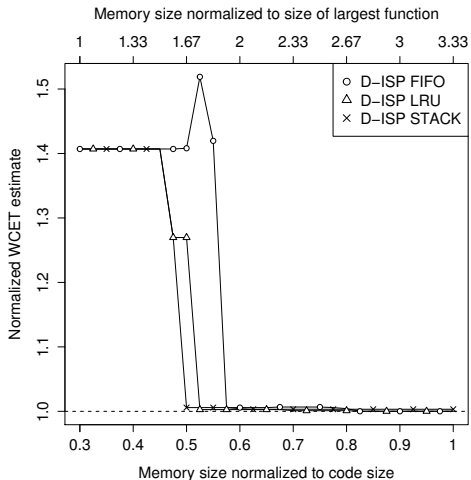


Quantification of the impact of the replacement policy on WCET estimate

- ▶ Static WCET analysis tool
  - ▶ Dual-issue in-order processor
  - ▶ Timing model of D-ISP with FIFO, Stack-based, and LRU replacement policy
  - ▶ D-ISP analysis using collective semantics
  - ▶ No on-chip data memory



- ▶ Benchmark: Sha
- ▶ FIFO with high eviction rate for small memory sizes
- ▶ Stack-based with few evictions for small sizes, but non-optimal behavior for large sizes



- ▶ Comparison of the hardware effort
- ▶ VHDL implementation of D-ISP controller with FIFO and stack-based replacement policy
- ▶ Synthesized for Altera Stratix II FPGA

<b>Replacement Policy</b>	<b>ALUTs</b>	<b>Registers</b>	<b>Max. f</b>
FIFO	809	613	103.17 MHz
Stack-based	995	643	101.21 MHz
Overhead of stack-based compared to FIFO (in %)	<b>+23.0%</b>	<b>+4.9%</b>	<b>-1.9%</b>

- ▶ Additional logic and register usage caused by different operation modes for call and return and their maintenance

## Conclusions

- ▶ Function-based instruction memory for HRT systems and the implementation of different replacement policies
- ▶ Comparison regarding WCET estimate & hardware effort
  - ▶ LRU: usually best WCET estimates, but not implementable
  - ▶ FIFO: lowest implementation cost, but high WCET estimates
  - ▶ Stack-based: with additional hardware effort than FIFO, WCET estimates comparable to LRU
- ▶ Future work
  - ▶ Development of scalable analysis techniques for function-based replacement policies